



## CE-ATA Technical Errata

|                            |                     |
|----------------------------|---------------------|
| <b>Errata ID</b>           | <b>Protocol 009</b> |
| <b>Affected Spec Ver.</b>  | <b>Protocol 1.0</b> |
| <b>Corrected Spec Ver.</b> |                     |

### Submission info

| Name          | Company | Date       |
|---------------|---------|------------|
| Amber Huffman | Intel   | 06/14/2005 |

### Description of the specification technical flaw (add space as needed)

The DD\_Cmd61W\_ChkCrc state goes back to DD\_Idle on a CRC error and ceases transmission for the corresponding RW\_MULTIPLE\_BLOCK (CMD61) command. It is important that an entire DRQ block be transferred from the host prior to ceasing MMC data line operations or the error cannot be accurately reflected to the host.

This erratum causes the MMC data layer to continue transferring data following a CRC error on a RW\_MULTIPLE\_BLOCK (CMD61) command. The MMC data layer will end a data transfer early if the device chooses to end the command by issuing the command completion signal.

Description of the correction

**The DD\_Cmd61W\_ChkCrc state in section 2.4.2.2.4 shall be modified as shown:**

|   |  |   |
|---|--|---|
| DD12:<br>DD_Cmd61W_ChkCrc   | Transmit positive CRC status of 010b on DAT0 if calculated CRC and received CRC are equal for all data lines, else transmit negative CRC status of 101b on DAT0. |   |
|   | 1. Calculated CRC and received CRC are equal for all data lines  | → DD_Cmd61W_ChkCnt                      |
|   | 2. Calculated CRC and received CRC are different for any data line   | → DD_Idle <sup>+</sup><br>DD_Cmd61W_Err |
| <b>NOTE:</b>  |  |   |
| 1. ATA layer is notified that RW_MULTIPLE_BLOCK (CMD61) was not completed successfully. |  |   |

**The DD\_Cmd61W\_Err state shall be added to section 2.4.2.2.4:**

|                      |  |                   |
|----------------------|--|-------------------|
| DD13b: DD_Cmd61W_Err | Notify ATA layer that MMC data block reception was not completed successfully.   |                   |
|                      | 1. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) not finished and ATA layer not ready to receive more data | → DD_Cmd61W_Bsy   |
|                      | 2. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) not finished and ATA layer is ready to receive data       | → DD_Cmd61W_Entry |
|                      | 3. Data transmission satisfying the Data Unit Count specified in RW_MULTIPLE_BLOCK (CMD61) finished  | → DD_Idle         |

**The DC\_Interrupt state in section 2.4.2.1 shall be modified as shown:**

|                   |   |           |
|-------------------|---|-----------|
| DC8: DC_Interrupt | Transmit a single '0' on the CMD line (the command completion signal). Notify MMC Data layer to stop any data transmission. |           |
|                   | 1. Unconditional  | → DC_Idle |

Disposition log

|            |                  |
|------------|------------------|
| 06/14/2005 | Erratum captured |
| 08/31/2005 | Erratum ratified |

Technical input submitted to the CE-ATA Workgroup is subject to the terms of the CE-ATA contributor's agreement.